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| 10/768,441 | 02/02/2004 | Hiroaki Nambu | 501.43352X00 | 1154 |

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| EXAMINER | |
|---|---|
| SUGENT, JAMES F | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/08/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/768,441 | NAMBU ET AL. | |
| | Examiner | Art Unit | |
| | James F. Sugent | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-10* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received December 1, 2006 for application number 10/768,441 originally filed February 2, 2004. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-10.

### *Claim Rejections - 35 USC § 103*

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al. (U.S. Patent No. 6,807,125 B2) (hereinafter referred to as Coteus) in view of Kashiwazaki (U.S. Patent No. 6,721,232 B2) (hereinafter referred to as Kashiwazaki).

As to claim 1, Coteus discloses a semiconductor integrated circuit comprising: a clock input terminal (13) for receiving a clock signal (DQS) and a data input terminal (12) for receiving a data signal (DQ) (column 2, lines 22-26); an internal clock generating circuit (19) for generating an internal clock signal (DQS_CLK and DQSN_CLK); a latch circuit (21 and 22) for latching the data signal input (DQ) to said data input terminal synchronously with said internal clock signal (Coteus discloses the incoming data being input into latches [21 and 22] are synchronized with the internal clocks [DQS_CLK and DQSN_CLK] as latch enable signals CLKS; column 2, lines 54-62); and, the internal clock comprising means for switching the internal clock signal at an intermediate timing between the i-th (i: an integer of 1 or larger)

switch timing and the (i+1)th switch timing of the clock signal input to said clock input terminal (as shown in figure 3) (Coteus discloses the internal clock generated [DQS_CLK] switches at an intermediate timing between the (i+1)th interval [90° out of phase]; column 2, lines 37-62).

Coteus fails to disclose a means for preventing a timing margin, at a time of latching the data signal synchronously with said internal clock signal, from being decreased in a case where a duty ratio of the clock signal input to the clock input terminal is different than 50%.

Kashiwazaki teaches a DLL circuit for a DDR SDRAM that comprises means for preventing a timing margin (DCC circuit 150), at a time of latching the data signal synchronously with said internal clock signal, from being decreased in a case where a duty ratio of the clock signal input to the clock input terminal is different than 50% (column 5, lines 29-65 and column 11, lines 21-34 and column 12, lines 8-29). Kashiwazaki also teaches the additional benefit of providing further techniques and device to overcome other timing issues present within an integrated circuit (column 4, lines 12-30).

It would have been obvious to one of ordinary skill of the art having the teachings of Coteus and Kashiwazaki at the time the invention was made, to modify internal clock generating circuit of Coteus to include the DCC circuit as taught by Kashiwazaki. One of ordinary skill in the art would be motivated to make this combination of including the DCC circuit within the internal clock generation circuit in view of the teachings of Kashiwazaki, as doing so would give the added benefit of providing further techniques and device to overcome other timing issues present within an integrated circuit (as taught by Kashiwazaki above).

As to claim 2, Coteus discloses the semiconductor integrated circuit wherein said internal clock generating circuit includes: first means (60) for holding a delay amount (DELAY_STEPS)

corresponding to time which is the half of the difference between the (i-j)th switch timing and the (i+1+j)th (j: an integer of 0 or larger) switch timing of the clock signal (an amount corresponding to switching of (2j+1) times) (Coteus discloses components 60 and 66 of the internal clock generating circuit [19] delaying the input clock [DQS] at a variable amount and therefore any fraction of said input clock DQS; column 4, line 54 thru column 6, line 10); and second means (66) for generating said internal clock by delaying said clock signal only by time of said held delay amount (column 4, line 54 thru column 6, line 10).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus (as cited above) and Kashiwazaki (as cited above) as applied to claim 1 above, and further in view of Kawasaki et al. (U.S. Patent No. 6,066,969) (hereinafter referred to as Kawasaki).

As to claim 3, Coteus fails to disclose the semiconductor integrated circuit wherein said internal clock generating circuit is comprised of first and second frequency dividers, a phase comparator, a variable delay circuit, and a delay control circuit and comprises: the first frequency divider for generating a first frequency divided signal synchronized with the (i-j)th switch timing of said clock signal; the second frequency divider for generating a second frequency divided signal synchronized with the (i+1+j)th switch timing of said clock signal; the phase comparator for comparing the phase of said first frequency divided signal and the phase of said second frequency divided signal; and the delay control circuit for controlling said variable delay circuit so as to have delay time corresponding to time which is the half of said phase difference, wherein said clock signal is input to the variable delay circuit, and an output signal of the variable delay circuit is used as said internal clock signal.

Kawasaki teaches a clock generating circuit [DLL figure 3] wherein said clock generating circuit is comprised of first (32) and second (31) frequency dividers, a phase comparator (33), a variable delay circuit (12), and a delay control circuit (18) and comprises: the first frequency divider (32) for generating a first frequency divided signal (dll-clk-div) (column 8, lines 50-59 and column 9, lines 23-35); the second frequency divider (31) for generating a second frequency divided signal (i-clk-div) (column 8, lines 50-59 and column 9, lines 23-35); the phase comparator (33) for comparing the phase of said first frequency divided signal (dll-clk-div) and the phase of said second frequency divided signal (i-clk-div) (column 8, lines 50-59); and the delay control circuit (18) for controlling said variable delay circuit (12) so as to have a variable delay time (Kawasaki discloses the delay control circuit setting a variable delay time dependent on the results of the phase comparator circuit [17]; column 7, lines 9-17 and column 7, lines 43-55), wherein said clock signal (i-clk) is input to the variable delay circuit (12), and an output signal of the variable delay circuit (dll-clk) is used as said internal clock signal (column 6, lines 37-41). Kawasaki also has the added feature of reducing excessive power consumption and shorten a time period required for achieving a lock-on condition when a clock signal switches from a longer cycle to a shorter cycle (column 3, lines 50-55).

It would have been obvious to one of ordinary skill of the art having the teachings of Coteus and Kawasaki at the time the invention was made, to modify the clock generating circuit of Coteus to include the DLL components as taught by Kawasaki such that the first frequency divider is synchronized with the (i-j)th switch timing of said clock signal, the second frequency divider is synchronized with the (i+1+j)th switch timing of said clock signal and the delay clock circuit has a delay time corresponding to time which is the half of said phase different. One of

ordinary skill in the art would be motivated to make this combination altering the clock generating circuit to include the DLL components in view of the teachings of Kawasaki, as doing so would give the added benefit of reducing excessive power consumption and shorten a time period required for achieving a lock-on condition when a clock signal switches from a longer cycle to a shorter cycle (column 3, lines 50-55).

As to claim 4, Kawasaki teaches the semiconductor integrated circuit further comprising a clock input buffer (11) for receiving a clock signal which is input to said clock input terminal, wherein said clock input buffer (in combination with the variable delay circuit 12) generates a first clock signal (dll-clk) and a second clock signal (i-clk) at a level complementary to the first clock signal (which can variably also be an inversion of the input clk), wherein, when the first clock signal (dll-clk) is input to said first frequency divider (32), the second clock signal (i-clk) is input to said second frequency divider (31), and wherein, when the first clock signal (dll-clk) is input to said second frequency divider (31), the second clock signal i-clk) is input to said first frequency divider (32) (column 8, lines 50-67).

***Allowable Subject Matter***

Claims 5-10 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The limitations found within independent claims 5 and 9 to include a semiconductor integrated circuit wherein the integrated circuit comprises an internal clock generating circuit and further comprises a means for preventing a timing margin, at a time of latching the data signal synchronously with said internal clock signal, from being decreased in a case where a duty ratio

of the clock signal input to the clock input terminal is different than 50%, said means including means for switching the internal clock signal at an intermediate timing between the i-th (i: an integer of 1 or larger) switch timing and the (i+l)th switch timing of the clock signal input to said clock input terminal wherein the means for preventing a timing margin further includes a first, second and third variable delay which have the same configuration; a first and second frequency divider wherein the first divider generates a first frequency divided signal that is synchronized with the (i-j)th switch timing of said clock signal and the second divider generates a second frequency divided signal that is synchronized with the (i+1+j)th switch timing of said clock signal; a phase comparator that compares the phases of the first and second frequency divided to obtain a phase difference; and, a delay control circuit that controls delay times of said first, second and third variable delay circuits so that the phase difference becomes zero could not be found, either singularly or in combination, in further Examiner's search and therefore deems dependent claims 6-8 and 10 allowable based on their dependence.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
January 26, 2007

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SUPERVISORY PATENT EXAMINER
2/3/07